CLAIMS

1. A digital-to-phase converter, comprising:

a delay line having a plurality of delay taps;

a multiplexor coupled to the delay line, the multiplexor having a plurality (N) of input ports for receiving the plurality of delay taps and an output port for providing an output signal; and

a synchronization circuit having a first input port for receiving the output signal from the multiplexor and a second input port for receiving a trigger signal, the synchronization circuit further having an output port for providing an output signal only when the synchronization circuit is gated by the trigger signal (TRIG).

2. A digital-to-phase converter as defined in claim 1, further comprising a reference clock signal having a time period and coupled to the delay line and the synchronization circuit, and wherein the delay line is tuned to a delay equal to the time period of the reference clock signal.

3. A digital-to-phase converter as defined in claim 1, wherein the plurality of delay taps on the delay line are equally spaced.

4. A digital-to-phase converter as defined in claim 1, wherein the delay line comprises an inverter chain where each inverter output represents a delay-line tap.

5. A digital-to-phase converter as defined in claim 4, further comprising a reference clock signal and the inverted version of the input clock signal represents the input clock shifted by 180 degrees plus the time delay of the delay line.

6. A digital-to-phase converter as defined in claim 1 wherein the delay line is slaved to a delay-line-loop (DLL).

7. A digital-to-phase converter as defined in claim 1, further comprising:

a reference clock providing a reference signal (REF) to the delay line and the synchronization circuit, and

the multiplexor includes an input port for receiving an n-bit binary word (IN).

8. A digital-to-phase converter as defined in claim 7, wherein the reference signal (REF) is a pulse train having rising and falling edges and the synchronization circuit forms multiple apertures that depend on the value of (IN).

9. A digital-to-phase converter as defined in claim 7, wherein the reference signal (REF) is a pulse train having rising and falling edges and the synchronization circuit forms an aperture region when IN <=N/2 that begins on the first rising edge of the reference signal (REF) after the first rising edge of the trigger signal (TRIG) signal and remains active for a predetermined period thereafter.

10. A digital-to-phase converter as defined in claim 9, wherein the predetermined period that the aperture region formed by the synchronization circuit remains active is approximately 3/2 the period (Tref) of the reference signal (REF).

11. A digital-to-phase converter as defined in claim 9, wherein the synchronization circuit forms an aperture region when IN >N/2 that begins on the first falling edge after the first rising edge of the reference signal (REF) after a trigger signal (TRIG) has occurred and the aperture region remains active for a predetermined period of time.

12. A digital-to-phase converter as defined in claim 11, wherein the predetermined period of time that the aperture remains active is for approximately 3/2 the period (Tref) of the reference signal.

13. A digital-to-phase converter, comprising:

a tuned delay line having a plurality of delay taps;

a multiplexor coupled to the delay line, the multiplexor having a plurality (N) of input ports for interconnecting with the plurality of delay taps on the tuned delay line and an output port for providing an output signal;

a synchronization circuit;

a reference clock providing a reference signal (REF) to the tuned delay line and the synchronization circuit; and

the delay line is tuned to a delay equal to the time period of the reference signal.

14. A digital-to-phase converter as defined in claim 13, wherein the delay line is adjusted using a delay-locked-loop (DLL).

15. A digital-to-phase converter as defined in claim 13, further comprising an output port coupled to the synchronization circuit and wherein the synchronization circuit provides a time aperture that allows the multiplexor's output signal to be presented at the output port of the synchronization circuit.

16. A digital-to-phase converter as defined in claim 13, wherein the delay taps are ordered so the fractional portion of the delay increases monotonically as the tap position number increases.